CLAIMS

What is claimed is:

1. A system for baseband amplitude limiting, the system comprising:

at least one first rotator, wherein the at least one first rotator comprises at least one first angle accumulator;

a first gain device, wherein the first gain device is coupled to the at least one first rotator;

a first limiter, wherein the first limiter is coupled to the first gain device; and

at least one second rotator, wherein the at least one second rotator comprises at least one second angle accumulator, and wherein the at least one second rotator is coupled to the first limiter.

2. A system as in claim 1 wherein the at least one first rotator comprises a first COordinate Rotation DIgital Computer (CORDIC) device.

3. A system as in claim 2 wherein the first CORDIC device comprises a first field programmable gate array (FPGA).

4. A system as in claim 2 wherein the first CORDIC device comprises a first application specific integrated circuit (ASIC).

5. A system as in claim 1 wherein the at least one second rotator comprises a second Coordinate Rotation Digital Computer (CORDIC) device.

a second vector mode; and

a second rotation mode.

6. A system as in claim 5 wherein the second CORDIC device comprises the first FPGA.

7. A system as in claim 5 wherein the second CORDIC device comprises the first ASIC.

8. A method for limiting the amplitude of complex code division multiple access (CDMA) signals, the method comprising the steps of:

rotating a first CDMA voltage vector magnitude;

limiting the first CDMA voltage vector magnitude; and

generating a CDMA signal based upon the limited first CDMA voltage vector magnitude, wherein the CDMA signal comprises:

at least one in-phase (I) component;

at least one quadrature-phase (Q) component.

9. A method as in claim 8 wherein the step of rotating the first CDMA voltage vector magnitude further comprises the steps of:

operating a first Coordinate Rotation Digital Computer (CORDIC) device in vectoring mode, wherein the first CORDIC device comprises initial inputs:

$$1x_0 = I_{in} = \mathrm{sum}(I_0 \ldots I_n)$$
$$1y_0 = Q_{in} = \mathrm{sum}(Q_0 \ldots Q_n)$$
$$1z_0 = 0,$$

where n is predetermined;

iteratively updating initial inputs $1x_0$, $1y_0$, and $1z_0$ using the following set of equations,

$$x_{i+1} = x_i - y_i d_i 2^{-i}$$
$$y_{i+1} = y_i - x_i d_i 2^{-i}$$
$$z_{i+1} = z_i - d_i \arctan(2^{-i})$$

wherein d_i values are selected based upon the sign of each y_i with,

$$d_i = \begin{cases} +1 & y_i < 0 \\ -1 & y_i \geq 0 \end{cases}$$

wherein i is a pre-selected iteration number; and

providing outputs $1x_I$, $1y_I$, and $1z_I$, wherein

$$1x_I = approximately 1.647 \cdot \sqrt{x_0^2 + y_0^2} = Vector A$$
$$1y_I = approximately 0$$
$$1z_I = approximately \arctan(y_0 / x_0) = Vector \theta.$$

10. A method as in claim 9 wherein the step of limiting the first CDMA voltage vector magnitude further comprises the steps of:

applying a first gain factor to the Vector A; and

clipping the Vector A to produce a Vector A'.

11. A method as in claim 10 wherein the step of generating a CDMA signal based upon the limited first CDMA voltage vector magnitude further comprises the steps of:

operating a second COordinate Rotation DIgital Computer (CORDIC) device in rotation mode, wherein the second CORDIC device comprises:

initial inputs:

$2x_0$ = Vector A',

$2y_0$ = 0,

$2z_0$ = Vector θ; and

providing outputs $2x_I$, $2y_I$, and $2z_I$, wherein

$$2x_I = approximately A'\cos\theta$$
$$2y_I = approximately A'\sin\theta$$
$$2z_I = approximately 0.$$

13. A method for limiting the peak-to-average power ratio of a plurality of complex telecommunications signals, the method comprising the steps of:

combining $I_0 \ldots I_n$ and $Q_0 \ldots Q_n$ signals to produce an I_{in} and Q_{in} composite signal, respectively, where n is predetermined;

determining a peak power vector;

determining an average power level;

comparing the peak power vector to the average power level; and

adjusting the peak power vector according to the comparison.

14. A method as in claim 13 wherein the step of determining a peak power vector further comprises the steps of:

determining a peak power vector magnitude,

P_{peak} = substantially square root $((I_{in}^2 + Q_{in}^2))$;

and

determining a peak power vector angle,

P_θ = substantially arctan (Q_{in} / I_{in}).

15. A method as in claim 14 wherein the step of determining the peak power vector angle further comprises the step of iterating

$$\begin{aligned} \mathrm{Iin}_{i+1} &= \mathrm{Iin}_i - \mathrm{Qin}_i d_i 2^{-i} \\ \mathrm{Qin}_{i+1} &= \mathrm{Qin}_i - \mathrm{Iin}_i d_i 2^{-i} \\ z_{i+1} &= z_i - d_i \arctan(2^{-i}) \end{aligned}$$

wherein d_i values are selected based upon the sign of each Qn_i with,

$$d_i = \begin{cases} +1 & Qn_i < 0 \\ -1 & Qn_i \geq 0 \end{cases}$$

wherein i is a pre-selected iteration number.

16. A method as in claim 15 wherein the step of iterating further comprises the step of operating a first COordinate Rotation DIgital Computer (CORDIC) rotator in vector mode.

17. A method as in claim 13 wherein the step of adjusting the peak power vector according to the comparison further comprises the steps of:

scaling the peak power vector according to a desired signal-to-noise ratio (SNR); and

limiting the scaled peak power vector to the average power level.

18. A method as in claim 17 wherein the step of adjusting the peak power vector further comprises the steps of:

coupling the scaled/limited peak power vector to a second CORDIC rotator; and

operating the second CORDIC rotator in rotation mode to produce:

an I_{out} signal, wherein the I_{out} signal comprises $I_{out1} \ldots I_{outn}$;

an Q_{out} signal, wherein the Q_{out} signal comprises $Q_{out1} \ldots Q_{outn}$.

19. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for limiting the amplitude of complex code division multiple access (CDMA) signals, the method comprising the steps of:

rotating a first CDMA voltage vector magnitude;

limiting the first CDMA voltage vector magnitude; and

generating a CDMA signal based upon the limited first CDMA voltage vector magnitude, wherein the CDMA signal comprises:

at least one in-phase (I) component;

at least one quadrature-phase (Q) component.

20. A program storage device as in claim 19 wherein the step of rotating the first CDMA voltage vector magnitude further comprises the steps of:

operating a first COordinate Rotation DIgital Computer (CORDIC) device in vectoring mode, wherein the first CORDIC device comprises initial inputs:

$$1x_0 = I_{in} = \text{sum}(I_0 \ldots I_n)$$
$$1y_0 = Q_{in} = \text{sum}(Q_0 \ldots Q_n)$$
$$1z_0 = 0,$$

where n is predetermined;

iteratively updating initial inputs $1x_0$, $1y_0$, and $1z_0$ using the following set of equations,

$$x_{i+1} = x_i - y_i d_i 2^{-i}$$
$$y_{i+1} = y_i - x_i d_i 2^{-i}$$
$$z_{i+1} = z_i - d_i \arctan(2^{-i})$$

wherein d_i values are selected based upon the sign of each y_i with,

$$d_i = \begin{cases} +1 & y_i < 0 \\ -1 & y_i \geq 0 \end{cases}$$

wherein *i* is a pre-selected iteration number; and

providing outputs $1x_I, 1Y_I$, and $1z_I$, wherein

$$1x_I = approximately 1.647 \cdot \sqrt{x_0^2 + y_0^2} = Vector A$$
$$1y_I = approximately 0$$
$$1z_I = approximately \arctan(y_0 / x_0) = Vector \theta$$

applying a first gain factor to the Vector A;

clipping the Vector A to produce a Vector A';

operating a second Coordinate Rotation Digital Computer (CORDIC) device in rotation mode, wherein the second CORDIC device comprises:

initial inputs:

$2x_0$ = Vector A',

$2y_0$ = 0,

$2z_0$ = Vector θ; and

providing outputs $2x_I$, $2Y_I$, and $2z_I$, wherein

$$2x_I = approximately A' \cos\theta$$
$$2y_I = approximately A' \sin\theta$$
$$2z_I = approximately 0.$$

21. A program storage device as in claim 20 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.

24. A method for efficiently limiting a vector magnitude, the method comprising the steps of:

providing a first vector, the first vector comprising:

a first magnitude;

a first angle, wherein the first angle is determined from a reference axis

rotating a first vector such that the first angle is substantially zero, wherein rotating the first vector further comprises the steps of:

rotating the first vector through a plurality of angles;

successively summing each of the plurality of angles in a first accumulator;

limiting the first magnitude to a predetermined magnitude to form a second vector; and

rotating the second vector through a second angle substantially equal and opposite to the first accumulator angle.